

# Design of Optimized 64 Bit MAC Unit for DSP Applications



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**Abstract :** A Design Of Optimized 64 Bit MULTIPLIER AND ACCUMULATOR (MAC) Unit Is Implemented In This Paper. MAC Unit Plays Major Role in Many Of The Digital Signal Processing (DSP) Applications. The MAC Unit Is Designed With The Combinations Of Multipliers And Adders. In the proposed Method MAC Unit Is Implemented Using Vedic Multiplier And The Adder Is Done With ripple Carry Adder .The Components Are Reduced By Implementing Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. A high speed processor depends significantly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. The Area Is Optimized Effectively Using Vedic Multiplier .The Total Design Implemented Using Xilinx .

**Keywords:** - MAC Operation, Vedic Mathematics (VM), Vedic Multiplier, Urdhava Tiryakbhyam Sutra , Ripple Carry Adder ,Multiplier And Accumulator (MAC).

## INTRODUCTION

MAC unit is MAC Unit Plays Major Role In Many Of The Digital Signal Processing (DSP) Applications. Involving multiplications and/or accumulations. MAC unit is used for best performance digital signal processing systems. The DSP applications include filtering, convolution, and inner products. Most of digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transforms (DWT)<sup>[1]</sup>. Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and accumulation arithmetic determines the execution speed and performance of the entire calculation. Multiplication-and-accumulate operations are typical for digital filters. Therefore, the functionality of the MAC unit enables high speed filtering and other processing typical for DSP applications. Since the MAC unit operates completely independent of the CPU, it can process data separately and thereby decrease CPU load. The application like optical communication systems

which is based on DSP require extremely high-speed processing of huge amount of digital data. The Fast Fourier Transform (FFT) also requires addition and multiplication. 64 bit can handle larger bits and have more memory<sup>[1]</sup>.

This paper is divided into six sections. In the first section the introduction about MAC unit is discussed. In the second section discuss about the detailed operation of MAC unit. The third section detailed about vedic mathematics and fourth section deals with the operation of Urdhva Tiryakbhyam Sutra of multiplication. In the fifth section obtained result for the 64 bit MAC unit is discussed and finally the conclusion is made in the sixth section.

## MAC OPERATION

The Multiplier-Accumulator (MAC) operation is the main key operation not only in DSP applications but also in multimedia information processing and various other applications. As mentioned above, MAC unit consist of multiplier, adder and register/accumulator<sup>[1]</sup>. In this paper, we used 64 bit Vedic multiplier. The multiply accumulate unit computes the product of two numbers and adds that product to an accumulator. The MAC unit consists of a multiplier followed by an adder and an accumulator register which stores the result<sup>[2]</sup>.

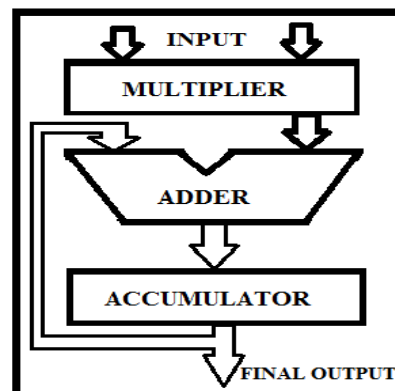


Fig 1 : Architecture of MAC unit

The architecture of the designed MAC unit is shown in the figure 1. The two input 64 bit operand to the MAC unit are A [63:0] and B [63:0]. The 64 bit output from MAC unit is Q[127:0]. The proposed design uses one 64x64 Vedic multiplier using Urdhva Tiryakbhyam algorithm. 128 bit accumulator using Ripple carry adder and one 128 bit register. Vedic multiplier design can increase MAC unit design speed and reduce the Area.

### VEDIC MATHEMATICS (VM)

The Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system<sup>[6]</sup>. Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers clarification of a number of modern mathematical terms including arithmetic, geometry, trigonometry, quadratic equations, factorization and constant calculus. His devotion Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. The very word "Veda" has the derivational meaning i.e. the source and limitless store housefull of knowledge<sup>[7]</sup>. Vedic mathematics is the name given to the prehistoric system of mathematics, to be precise a exclusive technique of calculations based on a simple rules and principle with which several mathematical problems can be solved, be it mathematics, algebra, geometry or trigonometry. The structure is based on 16 Vedic sutras or aphorisms, which are really word formula relating natural ways of solving a whole range of mathematical problems<sup>[3]</sup>. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human being mind works<sup>[6]</sup>. This is really interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. Vedic multiplication based on some algorithms are discussed below.

The 16 Sutras along with their briefly meanings are listed below alphabetically.

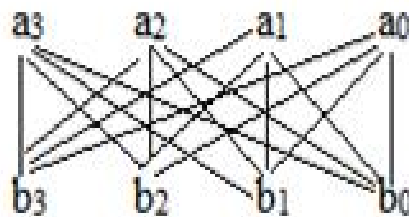
- 1) (Anurupy) Shunyamanyat -If one is in ratio, and the other one is zero.
- 2) ChalanaKalanabyham - Differences and similarities.

- 3) Ekadhikina Purvena- By one more than the previous One.
- 4) Ekanyunena Purvena -By one less than the previous one.
- 5) Gunakasamuchyah-Factors of the sum is equal to the sum of factors.
- 6) Gunitasamuchyah-The product of sum is equal to sum of the product.
- 7) Nikhila Navatashcaramam Dashatah -All from 9 and last from 10.
- 8) Paraavartya Yojayet-Transpose and adjust.
- 9) Puranapuranyam -By the completion or noncompletion.
- 10) Sankalana- vyavakalanabyam -By addition and by subtraction.
- 11) Shesanyakena Charamena- The remainders by the last digit.
- 12) Shunyam Saamyasamuccaye -When the sum is same then sum is zero.
- 13) Sopaantyadvayamantyam -The ultimate and twice the penultimate.
- 14) Urdhva-tiryakbhyam -Vertically and crosswise.
- 15) Vyashtisamanstih -Part and Whole.
- 16) Yaavadunam - Whatever the extent of its deficiency.

### Urdhva Tiryakbhyam Sutra

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a common multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a unique concept from first to last which the generation of all partial products can be done with the concurrent addition of these partial products shown in the fig 2. Therefore it is time, area and power optimized. Power dissipation which results in higher device operating temperatures. It is confirmed that this design is quite efficient in terms of silicon area/speed<sup>[5]</sup>.

Illustration for multiplication of two 4 - bit numbers



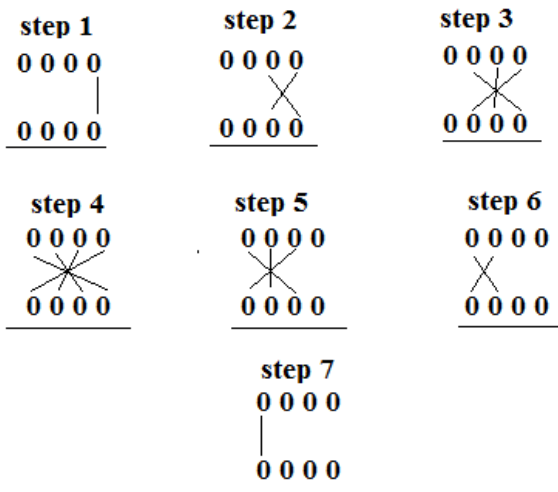
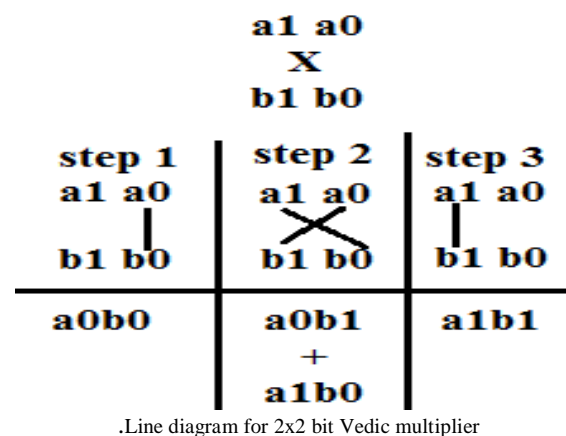


Fig 2.Line diagram for multiplication of two 4 - bit numbers

**Vedic Multiplier for 2x2 bit Module**

The method is explained below for two, 2 bit numbers A and B where  $A = a1a0$  and  $B = b1b0$ . Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and additional with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the MSB to give the sum and carry. The sum is the third equivalent bit and carry become the fourth bit Of the final product. The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram (Fig 3). It is found that the hardware design of 2x2 bit Vedic multiplier is same as the hardware design of 2x2 bit conventional Array Multiplier. Hence it is concluded that multiplication of 2 bit binary numbers by Vedic method does not made important effect in enhancement of the multipliers efficiency. Very accurately we can state that the total delay is only 2-half adder delays, after final bit products is generated, which is exactly same as Array multiplier<sup>[3]</sup>. So we switch over to the execution of 4x4 bit Vedic multiplier which uses the 2x2 bit multiplier as a basic structural block. The same method can be extended for input bits 4 & 8. But for higher number of bits in input, slightly

modification is required<sup>[3]</sup>.



.Line diagram for 2x2 bit Vedic multiplier

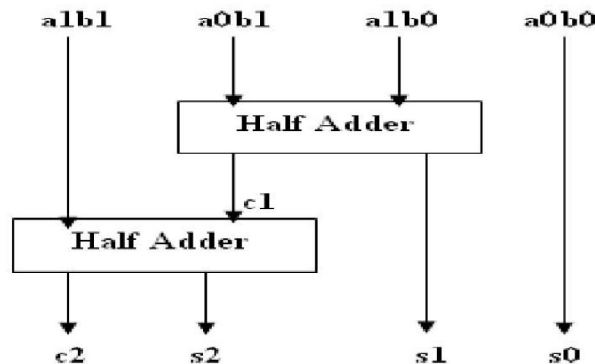


Fig 3.Block Diagram for 2X2 bit Vedic Multiplier

**Vedic Multiplier for 4x4 bit Module**

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Fig. 3. Let's analyze 4x4 multiplications, say  $A = A3 A2 A1 A0$  and  $B = B3 B2 B1 B0$ . The output of the multiplication result is  $S7 S6 S5 S4 S3 S2 S1 S0$ . Lets divide A and B divided into two parts, say  $A3 A2$  &  $A1 A0$  for A and  $B3 B2$  &  $B1 B0$  for B. Using the basic of Vedic multiplication, and taking two bit at a time and using 2 bit multiplier block, we can have the following structure for multiplication as shown in Fig. 4.

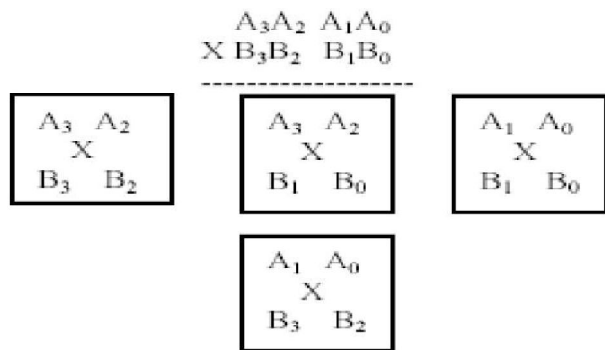


Fig. 4 Simple Representation for 4x4 bit Vedic Multiplication

Each block as shown above is 2x2 bit Vedic multiplier. First 2x2 bit multiplier inputs are A1 A0 and B1 B0. The last block is 2x2 bit multiplier with inputs A3 A2 and B3 B2. The middle one shows two 2x2 bit multiplier with inputs A3 A2 & B1 B0 and A1 A0 & B3 B2. So the final product of multiplication, which is of 8 bit, S7 S6 S5 S4 S3 S2 S1 S0. To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is shown in Fig5. To get final product (S7 S6 S5 S4 S3 S2 S1 S0), four 2x2 bit Vedic multiplier (Fig. 4) and three 4-bit Ripple-Carry (RC) Adders are required. The Vedic multiplier can be used to reduce ,area & power. we proposed a new architecture, which is efficient in terms of speed & power. The arrangements of RC Adders shown in Fig. 5, helps us to reduce delay. Interestingly, 8X8 Vedic multiplier module are implemented easily by using four 4x4 multiplier modules

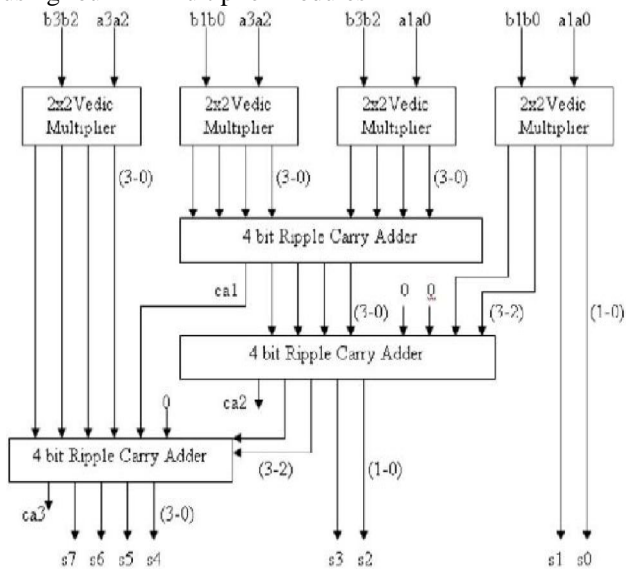


Fig. 5 Block Diagram of 4x4 bit Vedic Multiplier

**Vedic Multiplier for 8x8 bit Module**

The 8x8 bit Vedic multiplier module as shown in the block diagram in Fig. 6 can be simply implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section Let's

analyze 8x8 multiplications, say A= A7 A6 A5 A4 A3 A2 A1 A0 and B= B7 B6 B5 B4 B3 B2 B1 B0. The output for the multiplication result will be of 16 bits as S15 S14 S13 S12 S11 S10 S9 S8 S7 S6 S5 S4 S3 S2 S1 S0. Let's A and B divided into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decayed into BH-BL. The 16 bit product can be written as: Using the basic of Vedic multiplication, taking 4 bits at a time and using 4 bit multiplier block as discuss we can perform the multiplication. The outputs of 4X4 bit multipliers is added consequently to get the final product. Here total Three 8 bit Ripple-Carry Adders are required as shown in Fig. 6.

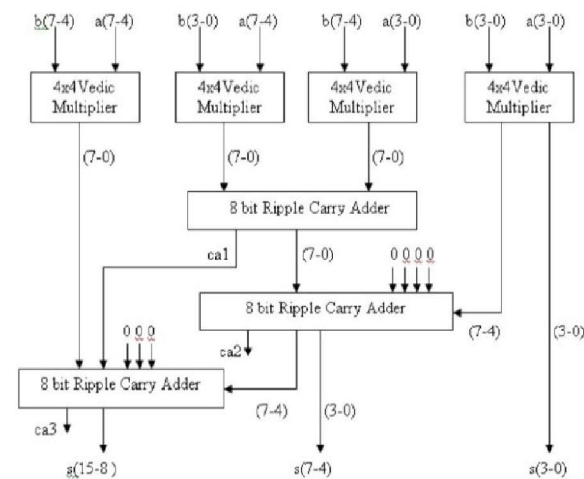


Fig. 6 Block Diagram of 8x8 bit Vedic Multiplier

**Generalized Algorithm for N x N bit Vedic Multiplier**

We can simplify the method as discussed in the before sections for any number of bits in input. Let, the multiplication of two N-bit binary numbers (where N = 1, 2, 3...N, must be in the form of 2N) A and B where A = AN....A3 A2 A1 A0 and B = BN....B3 B2 B1 B0. The final multiplication product will be of (N + N) bits as S = S(N + N)....S3 S2 S1 S0.

**Step 1:** Divide the multiplicand (A) and multiplier (B) into two equal parts, each consisting of [N to (N/2)+1] bits and [N/2 to1] bits respectively, where first part indicates the MSB and other represents LSB.

**Step 2:** Represent the parts of A as AM & AL, and parts of B as BM & BL. Now represent A and B as AM AL and BM BL respectively.



Power	WALLACE MAC	VEDIC MAC
LEAKAGE POWER (W)	0.175	0.165

**Step 3:** For A X B, we have general format as shown in Fig.7

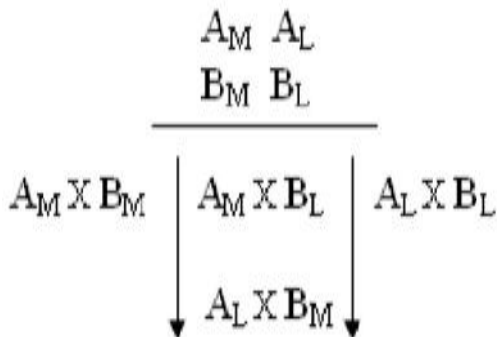
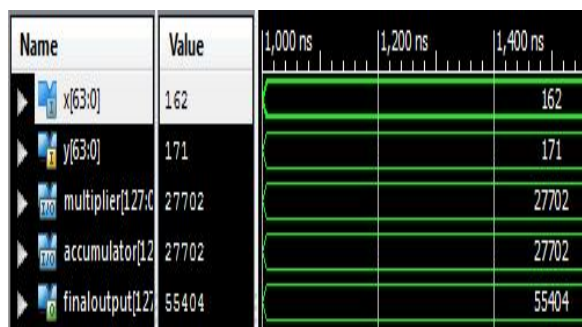


Fig.7 General Representation for Vedic multiplication

**RESULTS COMPARISION**

The design is developed using VHDL,And The previous work 64 bit MAC unit is designed using Modified Wallace multiplier<sup>[4]</sup>. The area, power dissipation comparative table are shown in the table 1 and table 2 respectively.

Simulation Waveform of 64 bit MAC unit



**Synthesis Report Of 64 Bit Mac Unit**

SYNTHESIS REPORT	WALLACE	VEDIC
NO.OF LUTS	239 OUT OF 10944 (2%)	129 OUT OF 10944 (1%)
NO OF SLICES	198 OUT OF 5472 (3%)	79 OUT OF 5472 (1%)
TOTAL NO OF LUTS	268 OUT OF 10944 (2%)	158 OUT OF 10944 (1%)
NO OF IOB'S	268 OUT OF 320 (85%)	256 OUT OF 320 (80%)

**Table1:** Comparison between 64-bit MAC Unit Of Using Wallace multiplier and Vedic multiplier.

**Table2:** Leakage Power Comparison Between 64-Bit Mac Unit Of Using Wallace Multiplier And Vedic Multiplier.

**CONCLUSION**

This paper presents a highly efficient optimized of MAC Unit Is Implemented Using Vedic Multiplier And The Adder Is Done With ripple Carry Adder . The Components Are Reduced By Implementing Vedic Multiplier using the techniques of “Urdhva Tiryakbhyam Sutra” based on Vedic mathematics is modified to improve performance. A high speed processor depends significantly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. The Area Is Optimized Effectively Using Vedic Multiplier .It is observed that the Vedic multiplier is much more efficient than Wallace multiplier in terms of Area. An awareness of Vedic mathematics can be effectively improved if it is integrated in Engineering Education.

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